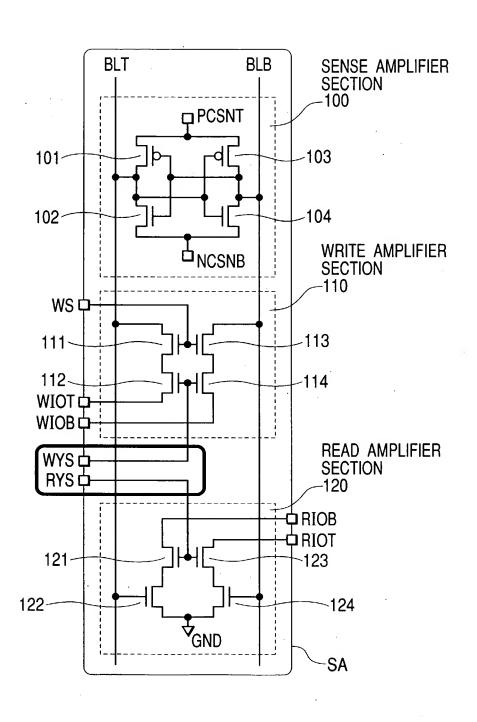


FIG. 1



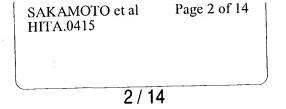
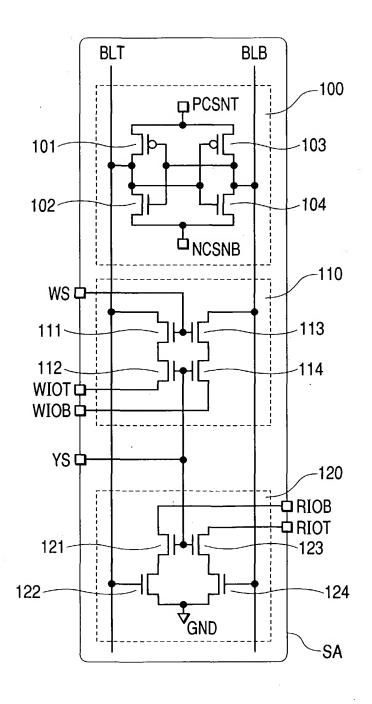
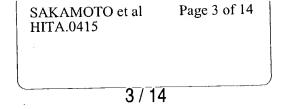
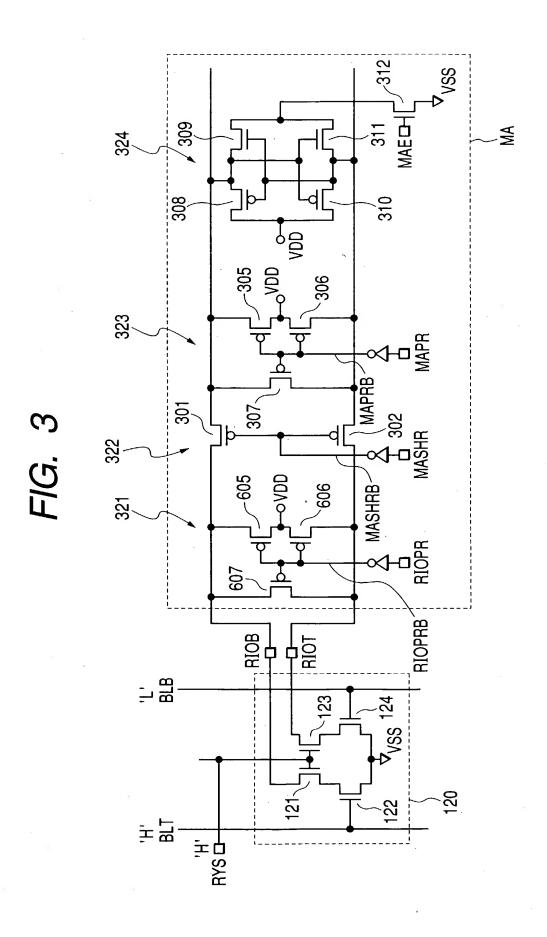
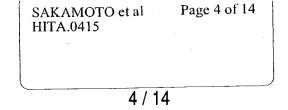


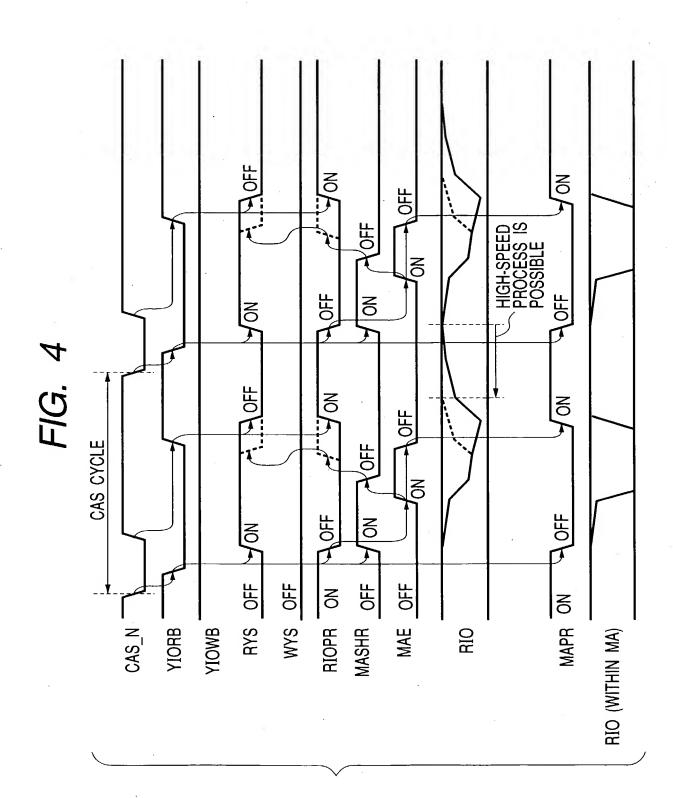
FIG. 2

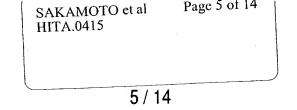


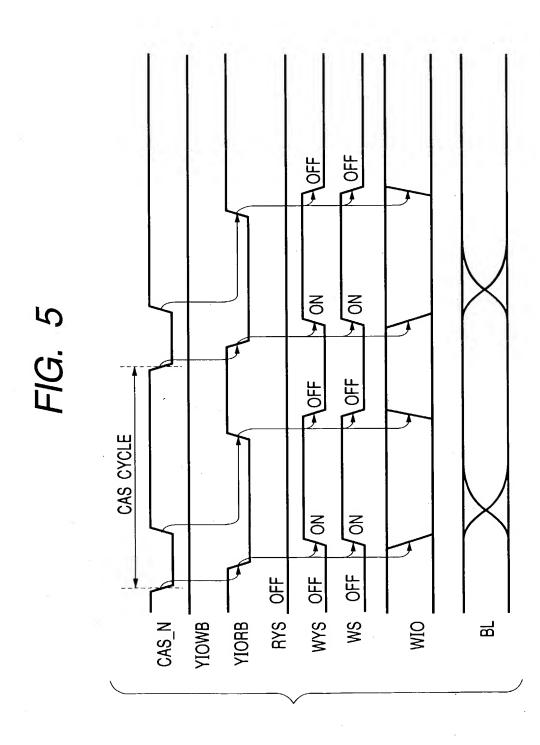












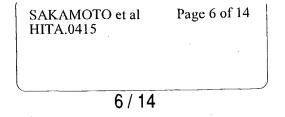


FIG. 6

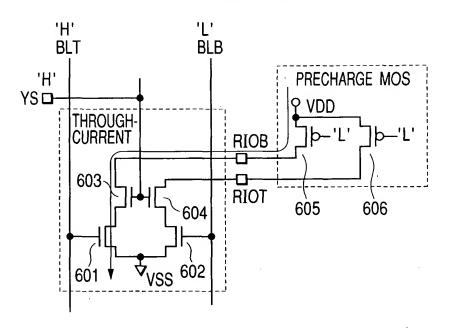
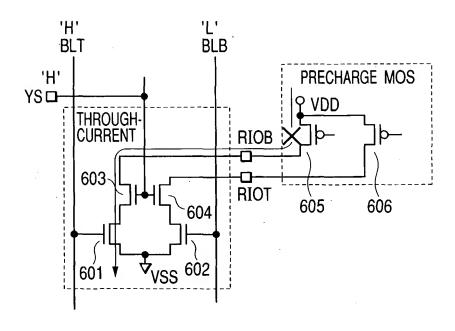
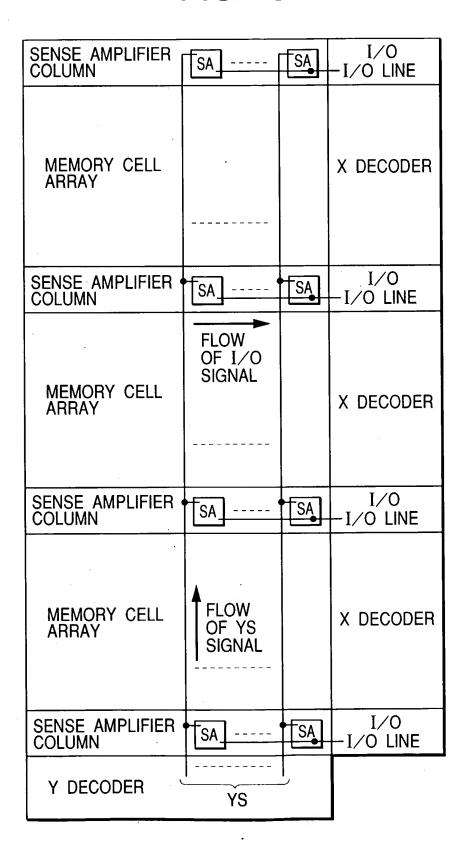


FIG. 7



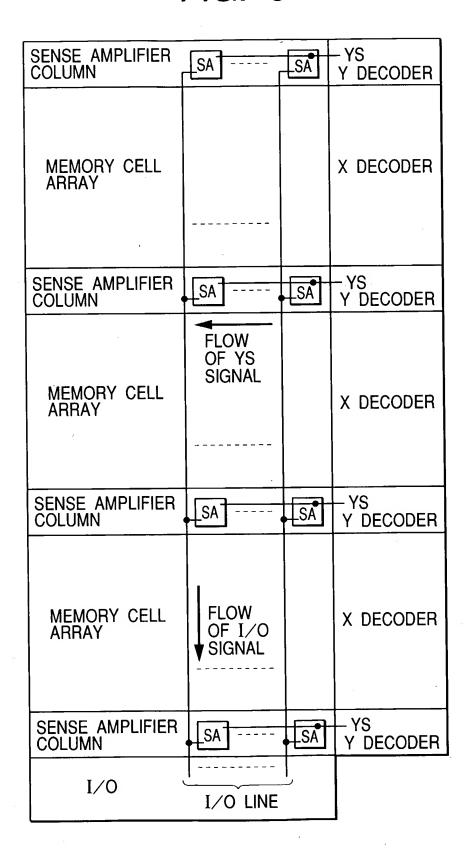
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FIG. 8



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FIG. 9



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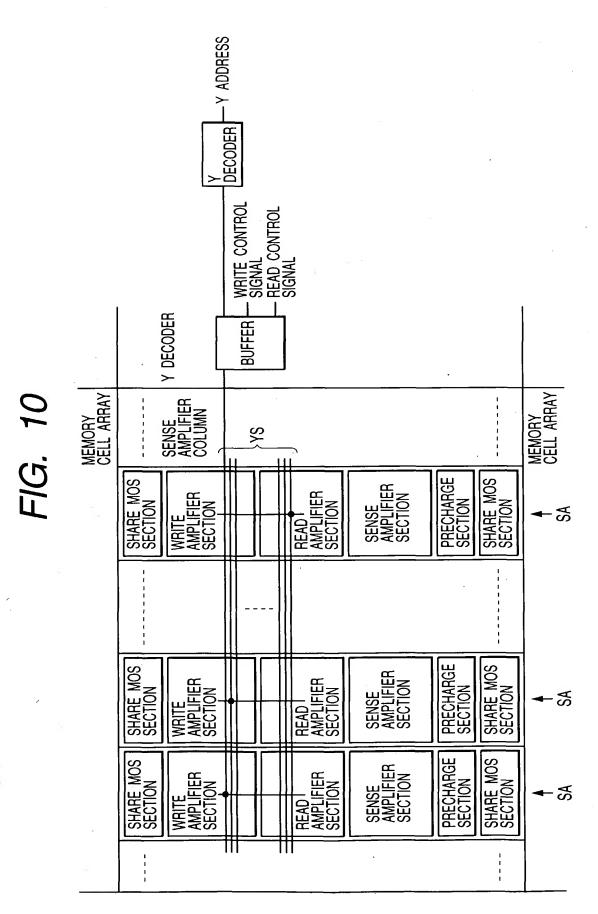
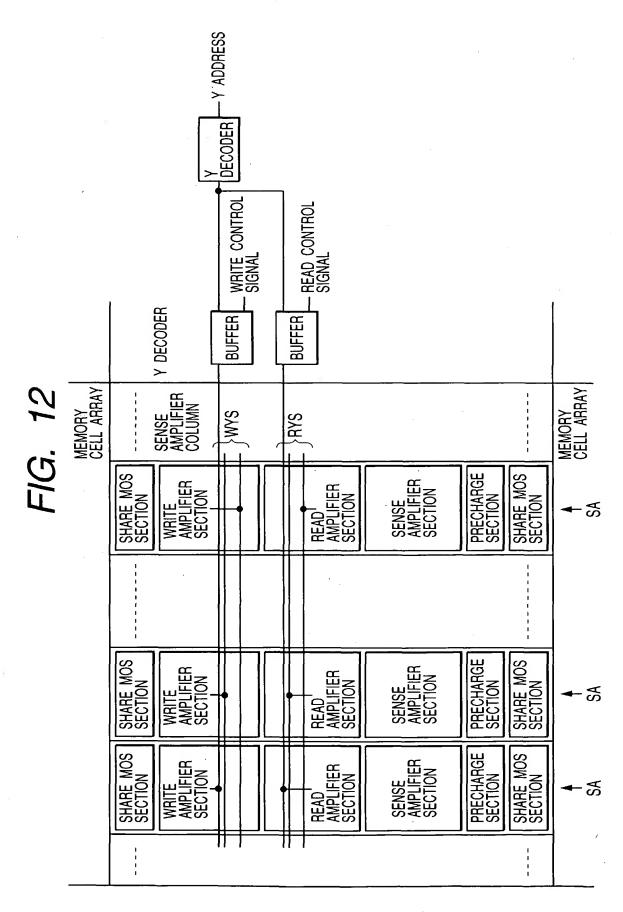
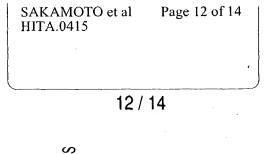


FIG. 11

MEMORY CELL ARRAY SAKAMOTO et al Page 11 of 14 HITA.0415





DECODER WRITE CONTROL SIGNAL - READ CONTROL SIGNAL Y DECODER BUFFER BUFFER FIG. 13 MEMORY CELL ARRAY \WXS \RYS SHARE MOS SECTION SHARE MOS SECTION WRITE AMPLIFIER SECTION -₩ SHARE MOS SECTION WRITE AMPLIFIER SECTION PRECHARGE SECTION SHARE MOS SECTION SHARE MOS SECTION SENSE AMPLIFIER SECTION WRITE AMPLIFIER SECTION READ' AMPLIFIER SECTION Sy-

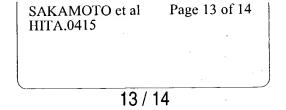


FIG. 14

